AMENDMENT TO THE SPECIFICATION

Please replace the third paragraph on page 12 with the following paragraph.

The memory read manager 400 includes a memory enable unit 410. The memory enable unit 410 is coupled to the read enable inputs of FIFO memories ~~331-334~~311-314. The memory enable unit 410 operates to transmit a read enable to the FIFO memories ~~331-334~~311-314. According to an embodiment of the memory read manager 400, the memory enable unit 410 tie asserts the read enable inputs of FIFO memories ~~331-334~~311-314 high such that the FIFO memories ~~331-334~~311-314 are always reading data.

Please replace the fifth paragraph on page 12 with the following paragraph.

The memory read manager 400 includes a read selector 430. The read selector 430 is coupled to the data output of the FIFO memories ~~331-334~~311-314. The read selector 430 selects data from the appropriate data output to pass through in response to the FIFO memory identified by the read address manager 420. According to an embodiment of the memory read manager 400 the read selector may pass the selected data to an output register.

Please replace the first paragraph on page 13 with the following paragraph.

The memory read manager 400 includes a plurality of read pointer managers 441-444. The read pointer managers 441-444 are coupled to the read address input of each of the FIFO memories ~~331-334~~311-314, respectively. The read pointer managers 441-444 operate to transmit an appropriate address to their respective FIFO memory in order to allow the FIFO memory to "pre-fetch" or prepare data for output prior to receiving an actual request for the data. According to an embodiment of the present invention, the read addresses transmitted to the FIFO memories

are initially set to zero. The read pointer managers 441-444 operate to increment the read address transmitted to the FIFO memories ~~331-334~~311-314 and to roll the read address back to zero.

Please replace the third paragraph on page 13 with the following paragraph.

The read side of the data buffering unit shown in Figure 4 is able to take advantage of the architecture of the FIFO memories ~~331-334~~311-314 and the fact that data is written into the FIFO memories ahead of time by a data transmitting device. By setting the read address of the FIFO memories ~~331-334~~311-314 to zero at intialization, and by tie asserting the read enable input of the FIFO memories ~~331-334~~311-314, data stored at address zero of FIFO memories ~~331-334~~311-314 may be prepared to be sent to the data output of the FIFO memories ~~331-334~~311-314 before any of the data is actually requested by the data reading device. When a read enable and read address are transmitted by the data reading device to request data from a FIFO memory, the FIFO memory may respond with the pre-fetched requested data within an acceptable period of time. The read pointer manager corresponding to the FIFO directs that FIFO memory to prepare a next data stored for output.